IN THE CLAIMS:

Please amend the claims as set forth below.

1. (Currently Amended) A mapper circuit for providing associations between logical registers and physical registers, the mapper circuit comprising a memory, the memory comprising:

a plurality of addressable units, each addressable unit addressed by a different logical register name (LRN) to which that addressable unit is statically assigned, and each addressable unit including a plurality of storage locations, wherein a first storage location of the plurality of storage locations is configured to store a current physical register name (PRN) currently assigned to the LRN, and wherein ~~one or more~~ each other storage ~~locations~~ location of the plurality of storage locations ~~are~~ is configured to store ~~one or more~~ an additional ~~PRNs~~ PRN previously assigned to the LRN; and

a control circuit coupled to the plurality of addressable units, wherein the control circuit is configured, responsive to a new PRN being assigned to a first LRN that addresses a first addressable unit of the plurality of addressable units, to cause the current PRN in the first storage location of the first addressable unit to be copied to a second storage location which is one of the other storage locations of the first addressable unit, wherein the second storage location corresponds to a current checkpoint of a plurality of checkpoints.

2. (Original) The mapper circuit as recited in claim 1, wherein the mapper circuit is configured to write the new PRN to the first storage location.

3. (Original) The mapper circuit as recited in claim 1, wherein the mapper circuit is configured to, responsive to a backup indication, revert the current PRN in the first storage location of each of the plurality of addressable units to the PRN from

one of the other storage locations, wherein the one of the other storage locations is indicated by the indication.

4. (Original) The mapper circuit as recited in claim 3, wherein the mapper circuit is coupled to receive a plurality of control signals, each corresponding to one of the storage locations, and wherein said reverting is performed by asserting one of the control signals.

5. (Original) The mapper circuit as recited in claim 4, wherein the backup indication is an insert pointer from a scheduler.

6. (Original) The mapper circuit as recited in claim 1, wherein the mapper circuit is configured make a copy the PRN in the first storage location to another one of the plurality of storage locations responsive to an assignment of new PRN for another LRN.

7. (Original) The mapper circuit as recited in claim 1, wherein the mapper circuit is coupled to receive a plurality of control signals, each corresponding to one of the other storage locations, and wherein the mapper circuit is configured to copy a PRN by asserting one of the plurality of control signals.

8. (Original) The mapper circuit as recited in claim 7, wherein the one of the plurality of control signals is asserted based on an insert pointer.

9. (Original) The mapper circuit as recited in claim 1, wherein the mapper circuit includes a read port for reading a PRN, wherein the address of the PRN is the desired LRN, and wherein the PRN is read from the first storage location of the addressable unit corresponding to the LRN, and wherein the mapper circuit is configured to output the corresponding PRN responsive to a read operation.

10. (Original) A mapper circuit for providing associations between logical registers and physical registers, the mapper circuit comprising a memory, the memory comprising:

a plurality of memory locations, each corresponding to a different physical register name (PRN), and wherein each memory location is configured to store a logical register name (LRN) and a plurality of valid indications, and wherein each of the valid indications corresponds to a checkpoint and is indicative of whether or not the PRN is assigned to the LRN at that checkpoint;

wherein a portion of the memory location storing the LRN is implemented as a content addressable memory (CAM) for comparison with an input LRN to the mapper circuit, and wherein a first PRN corresponding to a first memory location of the plurality of memory locations is output as a mapping of the input LRN if the LRN in the first memory location matches the input LRN and a first valid indication of the plurality of valid indications that corresponds a current checkpoint indicates that the first PRN is assigned to that LRN at the current checkpoint.

11. (Original) The mapper circuit as recited in claim 10, first valid indication is stored in a fixed location.

12. (Original) The mapper circuit as recited in claim 10, wherein a location of the first valid indication is indicated by a pointer.

13. (Original) The mapper circuit as recited in claim 10, wherein the mapper circuit includes a write port, wherein when a new PRN is assigned to an LRN, the PRN assigned to the LRN is the address on the write port where data is to be written, and wherein the LRN is the data that is written.

14. (Original) The mapper circuit as recited in claim 13, wherein a valid bit corresponding to the LRN is set responsive to the LRN being assigned to a new PRN at a new checkpoint.

15. (Original) The mapper circuit as recited in claim 13, wherein, if an LRN is not assigned to the first PRN for the current checkpoint but was assigned to the first PRN for a previous checkpoint, the valid bit is reset.

16. (Original) The mapper circuit as recited in claim 15, wherein, if an LRN is assigned to the first PRN for the current checkpoint and was assigned to the first LRN for the previous checkpoint, wherein the previous checkpoint is associated with a last speculative state existing before a speculative state corresponding to the current checkpoint, the valid bit from the previous checkpoint is copied to the current checkpoint.

17. (Original) The mapper circuit as recited in claim 16, wherein, if an LRN is not assigned to the first PRN for the current checkpoint but was assigned to the first PRN for the previous checkpoint, the valid bit is reset.

18. (New) The mapper circuit as recited in claim 1, wherein the control circuit is further configured to cause the current PRN in each of the other ones of the addressable units to be copied to one of the other storage locations that corresponds to the current checkpoint.

19. (New) The mapper circuit as recited in claim 1, wherein the memory circuit is arranged into a plurality of rows and a plurality of columns, wherein each row corresponds to an LRN and wherein each column corresponds to one of the plurality of checkpoints, and wherein a PRN is stored in each of the storage locations, thereby associating a PRN to an LRN for a given one of the plurality of checkpoints.